Approval: 10th Senate Meeting

Course number: EE 519 P

Course name: CMOS Digital IC design Practicum

Credit: 1-0-2-2 (L-T-P-C)

Intended for: MTech

Elective or Core: Core

Prerequisites: None

Semester: Odd

Preamble: The practicum course will cover the analysis and the design of CMOS digital integrated circuits considering the applications such as memories (DRAM, SRAM, DDR), processor design. The experiments include models of wires, capacitive coupling, inverter design, the design of combinational gates, sequential circuits using CMOS technology. The objective will cover the concept of the understanding of signal integrity. The course deals with extensive usage of Cadence Spectre, MentorGraphics Eldo for the schematic, the simulations and the layout design including parasitic extracted capacitors and inductors at various frequencies, PCB design using Cadence's Allegro and Xilinx FPGA boads.

Course Content

All the experiments will be performed using a standard 180 nm CMOS technology, provided by SCL Chandigarh or a smaller technology node.

Module: 1 (Physics and modeling of MOS transistor) [2 lectures + 2 laboratory hours]

- MOS Device understanding, NGSPICE and PSPICE modeling
- Introduction to industry standard tools such as Cadence's Virtuoso schematic, Spectre/Eldo simulator,

Module: 2 (Digital design and simulations) [2 lectures + 4 laboratory hours]

- MOSFET device characteristics using NGSPICE and Cadence's Virtuoso schematic and Spectre/Eldo simulators.
- Design of CMOS inverter for a given load and generation of I/O characteristics, gain and bandwidth measurement.

Module: 3 (Layout design techniques and methodologies) [2 lectures + 2 laboratory hours]

- Design rule, antenna effects, multi-finger transistor, passive device layout and inter connects

- Layout of CMOS inverter – design rule check(DRC) and layout v/s schematic (LVS). Post layout simulation (PLS) using Calibre of MentorGraphics of CMOS inverter using understanding of parasitics R, L and C.

Module: 4 (**Design, layout and PLS of combinational logic circuits) [2 lectures + 6 laboratory hours]**

Design, layout and PLS of CMOS digital functions using Complementary CMOS, Pass transistor, Pseudo NMOS logic, Complementary Pass Transistor Logic.

- Design, layout and PLS of multiplexer and demultiplexer.

Module: 3 (Design, layout and PLS of sequential logic circuits) [2 lectures + 6 laboratory hours]

- Design, layout and PLS of sequential logic circuits.
- Finite state machine implementation (FSM)

Module: 4 (Memory design) [2 lectures + 4 laboratory hours]

- Design, layout and PLS of memory unit cell, and the complete memory. Learning of GDS generation generation.
- The students will submit the project on memory using industry standard tools. The students will follow all the steps from schematic entry to GDS file generation.

Module: 5 (FPGA) [2 lectures + 4 laboratory hours]

- Introduction to FPGA. Hand-on sessions on XILINX FPGA kits.

Reference books:

1. "CMOS VLSI Design A Circuits and Systems Perspective" by Neil H. E. Weste and D. Harris.
2. "Digital Integrated Circuits" by J. Rabaey.